Name .....Nishant..... Entry No:.....1182.....

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INDIAN INSTITUTE OF TECHNOLOGY ROPAR

EE 203 Digital Circuits

First Semester of Academic Year 2023 - 2024

Mid semester Examination

Duration:2 Hours | Max. Marks: 50 | Date:21-09-2023

Instructions:

- Use of scientific calculator is allowed. Solve the questions with procedure.

Q1. (a) Using 10's complement subtract 72532 – 3250. 3 Marks

(b) Given two binary number X= 1010100 and Y= 1000011, Perform the subtraction Y – X, using 2's complement. 3 Marks

Q2. (a) Determine the base of the numbers for the following operation to be correct.

$24 + 17 = 40$ 3 Marks

(b) Show that A'BD' + BCD + ABC' + AB'D = BC'D' + AD + A'BC 3 Marks

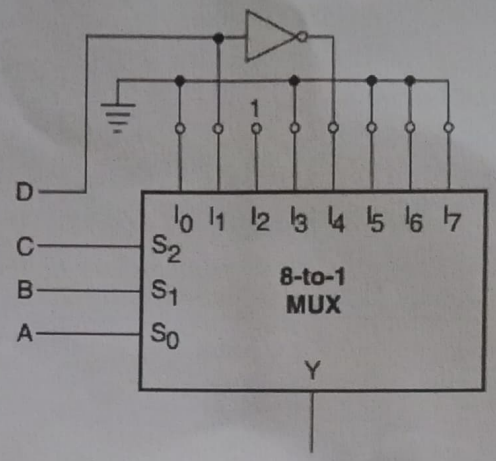
(c) Simplify the following Boolean expression:

A'BC + AB'C' + A'B'C' + AB'C + ABC 3 Marks

Q3. The four inputs to a network (P, Q, R, S) represent an 8421 binary-coded decimal (BCD) digit. Design (Simplify the expression using K-map and logic gates) the network so that the output is one if the decimal number represented by the inputs is exactly divisible by 3. Assume that valid BCD digits occur as inputs. 6 Marks

Q4. (a) Design a combination circuit for 4-bit Binary to Gray code converter (Simplify the expression using K-map and implement the circuit using logic gates). 6 Marks

(b) Figure shows the use of an 8-to-1 multiplexer to implement a certain four-variable Boolean function. From the given logic circuit arrangement, derive the Boolean expression implemented by the given circuit. 6 Marks



Q5. Find the minimized expression for the Boolean function:

F (W, X, Y, Z) = ∏ M (0,1,4,5,8,9,11) + Don't care (2,10) 5 Marks

Q6. Construct a 5-to-16-line decoder with five 2-to-4-line decoder with enable. 5 Marks

Q7. Let us assume that in J.C. Bose Block, IIT Ropar building combination locks are used to control entry. As the design engineer of the PQ security company, you are asked to implement a door security system by using a card reader. There are four inputs to the card reader: input A, B, and C is used to validate the correct door code, and input V is used to check if the card reader is still valid. After the card reader is being read by the system, there are three outputs to this system: alarm (X), door open (Y), and Error (Z). Door (Y) will only open when the decimal value of the binary inputs (A, B, C) is odd AND the card reader is valid. The error signal (Z) goes on when the code on the card is correct (i.e. decimal value equal to odd) but the card is no longer valid. Finally, the alarm (X) will trigger when the code is incorrect. Show the final design in canonical product of sum form (Using K-Map only) and implement the expression using logic gates. 7 Marks

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*****End*****

Name ..Nisha..... Entry No:.....192.....

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INDIAN INSTITUTE OF TECHNOLOGY ROPAR

EE 203 Digital Circuits

First Semester of Academic Year 2023 - 2024

End semester Examination

Duration: 3 Hours | Max. Marks: 50 | Date:23-11-2023

Instructions:

- Use of scientific calculator is allowed. Solve the questions with procedure.

Q1. (a) Convert $(110100111.01)_2$ to octal base and then to decimal. 3 Marks

(b) Convert $(756.603)_8$ to hexadecimal base. 2 Marks

Q2. (a) Subtract the 416.73 – 2928.54 using 10's complement method. 2 Marks

(b) Show that AB + AB'C + BC' = AC + BC' 2 Marks

Q3. Design a combinational circuit to produce the 2's complement of a 4-bit binary number (Simplify the expression using K-map). 5 Marks

Q4. Find the minimized sum-of-product expression for the Boolean function and implement the function using logic gates:

$F(A,B,C,D,E) = \sum m(0,2,6,7,8,10,11,12,13,14,16,18,19,29,30) + \text{Don't care } (4,9,21)$ 5 Marks

Q5. Design a counter using J-K flip-flop that goes through the following states 0, 2, 4, 6, 7, 0... Avoid the lockout condition. 6 Marks

Q6. Design a 2-4-2-1 weighted code base up-down counter that uses control signal for up and down counting. 6 Marks

Q7. (a) Draw the circuit diagram and explain the working of 3 input NAND gate using DTL.

(b) Draw the circuit diagram and explain the working of 2 input CMOS NOR gate. 3x2=6 Marks

Q8. Draw the circuit diagram and explain the working of R-2R ladder digital to analog converter. Find out the output voltage for binary number 1000. Consider for logic '1' output is 5V and for logic '0' as 0V. 5 Marks

Q9. (a) Draw the circuit diagram of DRAM and explain the working. 4 Marks

(b) Draw the circuit and explain the working of counter type ADC converter. 4 Marks

*****End*****